RECEIVED
CENTRAL FAX CENTER
NOV 10 2009

Application No.: 10/593,280

AMENDMENTS TO THE SPECIFICATION

Please amend the abstract of the instant application as follows:

ABSTRACT OF THE DISCLOSURE

~~When a storage circuit (13) of a certain stage and those of the following stages are caused to stop, a storage element circuit (11) of a memory area B (2) that stores survivor paths of a particular state is caused to serve as a repeater, and the other storage element circuits (11), which belong to a memory area C (3) are caused to stop, whereby a decoding result can be outputted without using additional bus wires and selectors.~~

A path memory circuit for use in a Viterbi decoding process performed based on state transitions through a number n (n is a positive integer) of states. The path memory circuit includes a memory area A formed by the storage circuits of the first to i^{th} (i is an integer from 0 to M) stages; a memory area B formed by the selective storage circuits that select and hold a decoding result for any state k (k is an integer from 1 to n) of the storage circuits from the $i+1^{th}$ stage to the M^{th} stage; and a memory area C formed by the selective storage circuits other than the memory area A and the memory area B.